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Advances in Data Handling Systems for Space Experiment Control

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The Space Vehicles Directorate of the U.S. Air Force Research Laboratory developed a small satellite payload package containing an ensemble of microelectronics subexperiments, which was integrated and launched on the Space Test Research Vehicle-1d satellite. The scientific payload consists of an electronics testbed, nine subexperiments, and a data handling system that in turn interfaces with the spacecraft onboard computer. The hardware and software architectures are described, and future extensions of the data handling system concept are discussed.

Introduction

A CONTINUING concern in the development of future spacecraft is the effect of the synergistic radiation environment on new forms of electronics and sensor technologies. Experimental opportunities to evaluate on-orbit performance are rare. Responding to such opportunities is problematic, due to the lack of an easy way for researchers to construct a small, effective payload that can effectively access satellite "services" (power, telemetry, command, and control). Such services are not usually in a form convenient to simple experiments, which might be concerned with basic measurements, such as the drift in the leakage current of a semiconductor device over time. As such, few payloads have been assembled to respond to investigative needs for combined radiation effects environments. Recent work with the U.S./U.K. Space Test Research Vehicle (STRV) series of satellites, however, has created precisely the type of electronics testbeds (ETBs) needed for such exploratory work on a scale and time frame accessible to ordinary researchers using relatively simple "plug-and-play" interface concepts. Most notably, in the Ballistic Missile Defense Organization (BMDO) sponsored ETB for STRV-1d, an efficient experimental payload ensemble consisting of a central data handling system and nine separately developed subexperiments has been established. The Space Vehicles Directorate of the U.S. Air Force Research Laboratory (AFRL) is managing, developing, and delivering this small payload (~3 kg for the ensemble) for integration into the STRV-1d satellite, which was launched with the STRV-1c companion spacecraft in autumn 2000. The STRV-1c and STRV-1d spacecraft were placed into highly elliptical orbits where they pass in and out of the Van Allen radiation belts every 10.5 h during their mission. The AFRL data-handling system (DHS) services three Department of Defense (DOD) experiments, five NASA experiments, and a Defense Research Establishment Ottawa (DREO) (Canadian) experiment.

This paper will detail the development and fabrication of an efficient DHS toward the end of establishing a plug-and-play space experiment "brokering" system. The DHS is a self-contained computer that provides a large number of general-purpose interface ports, analog sampling, isolated power conversion, and expanded memory management capability. The DHS design simplifies some of the complexities to be faced by individual subexperimenters by providing a less complex interface for operation and measurement of advanced electronics radiation performance in the harsh STRV-1d space environment. The DHS improves on-orbit use of individual subexperiment resources by recording experimental results, storing them locally, and then communicating those results to the spacecraft for download to the ground station. The DHS reduces the risk to the spacecraft mission by providing a degree of separation between the spacecraft and less-proven new technologies contained in each experiment and by providing a similar degree of separation between the experiments. In the process of developing the ETB DHS, a simple 12-conductor interface was employed. This interface was based on the RS-422 signaling standard, along with standardized definitions for supply voltage and analog inputs. This interface was developed so that it can be used on future space missions. When various novel approaches to the design aspects and requirements are used, a high functionality was reached while preserving valuable spacecraft power and mass, which allowed additional experiments to be manifested.

Moving further toward the goal of the ideal no-weight and no-power DHS, future ETB architectures are described in the paper that surpass the efficiency in size, mass, and power of the present design. This includes a peer-to-peer distributed ETB concept, which does not require a centralized DHS.

ETB Description

The ETBs in the STRV series are designed to permit a capability for evaluating a set of subexperiments that represent various emerging electronics and sensor technologies as they operate in a realistic space environment. The ETBs do not replace but supplement extensive ground-testing programs in available radiation sources worldwide. The ETBs contribute not only a legacy for qualification procedure development, but also a unique synergistic space environment that cannot be matched by any ordinary ground-test facility. New insights are expected in the development, integration, and operation of these experiments, which may lead to improvements in future satellite programs.

ETB Subexperiments

The STRV-1d ETB, symbolically shown in Fig. 1, is configured to support nine external subexperiments. These experiments are "laundered" through the DHS to the spacecraft. More than that, the DHS provides conditioned power, command and control, analog measurement, and telemetry support, while protecting the spacecraft and other peer subexperiments from the consequences of failed subexperiments. Summary descriptions of the current subexperiment manifest of the STRV-1d ETB follow.

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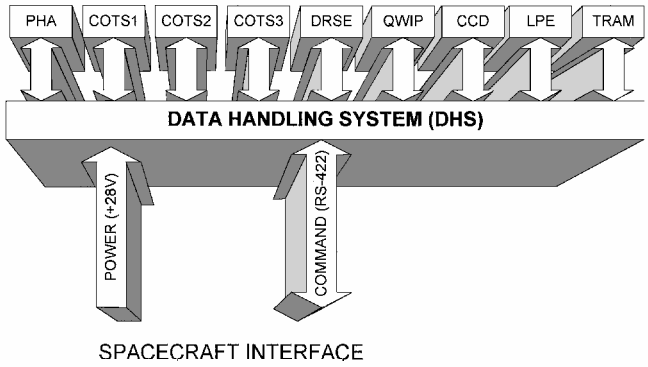


Fig. 1 ETB experiment on STRV-1d.

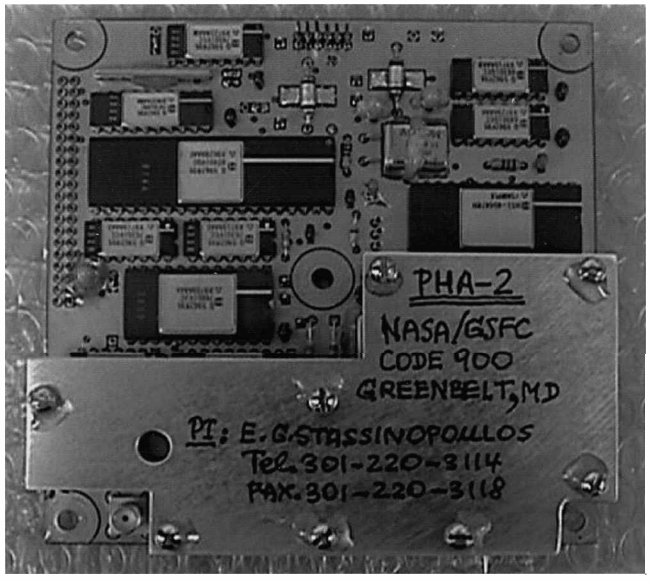


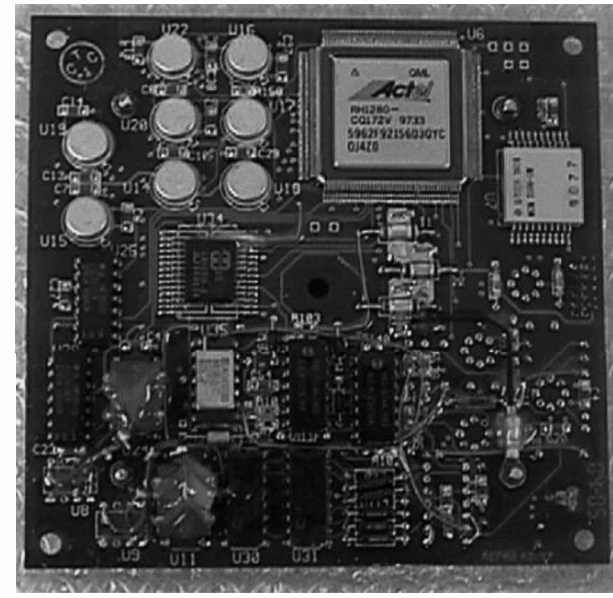
Fig. 2 NASA PHA subexperiment with radiation shield covering lower section of electronics.

Pulse-Height Analyzer (NASA)

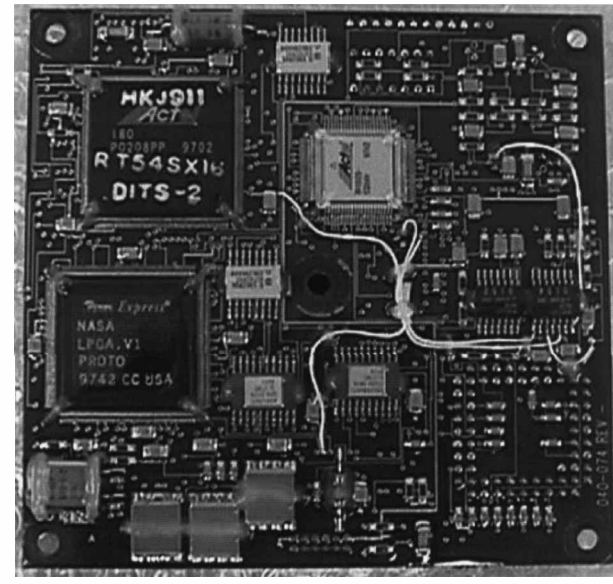
The pulse-height analyzer (PHA) is one of two ETB subexperiments dedicated to improved dosimetry, in this case to establish measurements of the linear energy transfer value, which is an important indicator in the study of single-event phenomena (SEP) in space-based microelectronics, especially those involving commercial off-the-shelf (COTS) devices. As a side benefit, the PHA instrument (Fig. 2) is sensitive to phenomenology associated with solar flares. The indication of solar flares, which will be correlated with other sources during operation, can be exploited by the DHS to trigger a special operating sequence designed to examine more closely the SEP-sensitive elements of other particular subexperiments.

COTS 1 (NASA)

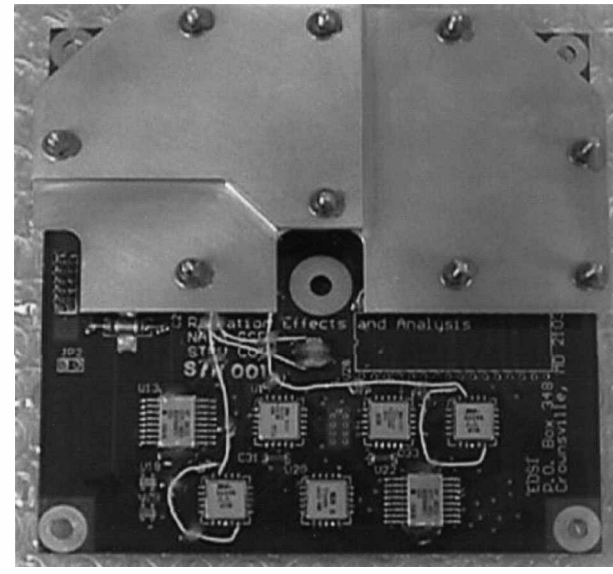
This subexperiment examines controversial elements of analog electronics in which the enhanced low dose rate effects (ELDRS) phenomena has been observed.[1] ELDRS effect refers to a dose-rate-dependant degradation in bipolar transistors fabricated in certain integrated circuit (IC) processes. The finding, which shows a greater damage at lower dose rates, is particularly controversial because 1) it may invalidate traditional radiation effects testing (normally done at much higher dose rates) and 2) the ELDRS effect may be more pronounced in natural space environments. COTS 1 (Fig. 3a) will be the first experiment dedicated to examining the ELDRS effect in a true space radiation environment. It will examine the degradation of LM109 comparators built in semiconductor processes suspected of having high susceptibility to the ELDRS effect. Verification of the ELDRS effect manifested in true space environments may drive a modified space qualification regimen in modern linear microcircuits.



a) COTS 1



b) COTS 2



c) COTS 3

Fig. 3 NASA COTS subexperiments.

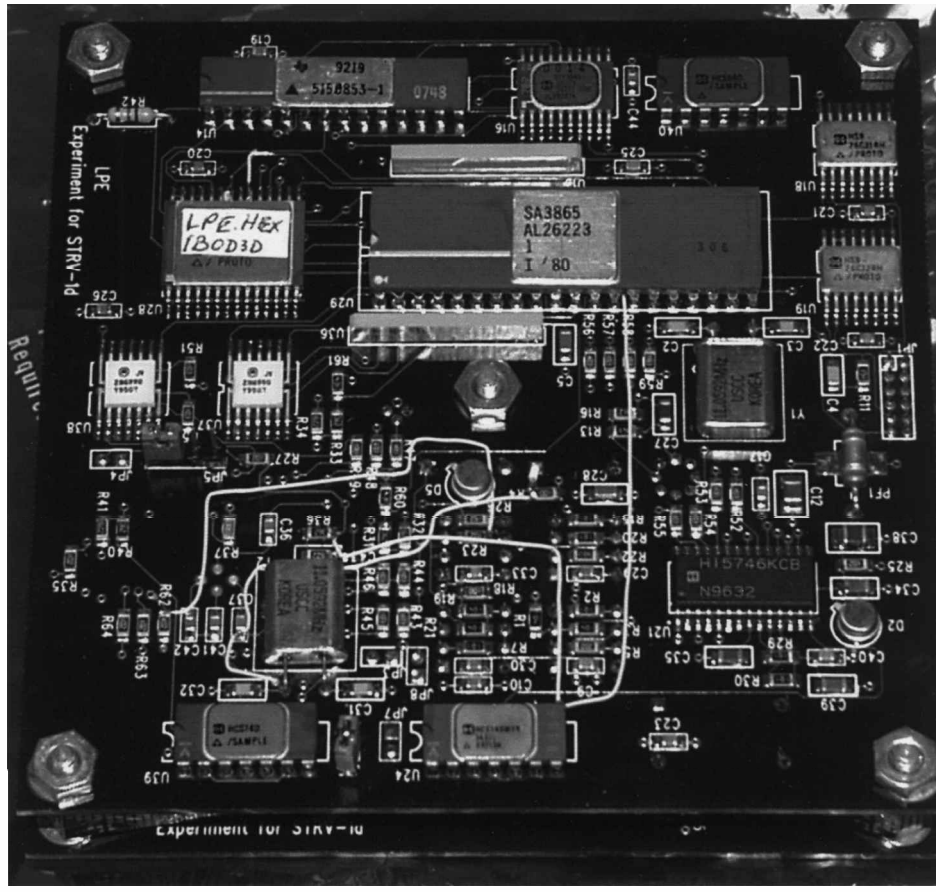


Fig. 4 LPE subexperiment.

COTS 2 (NASA)

This subexperiment will examine synergistic radiation effects on a variety of newer state-of-the-artdigital microcircuit and multichip module (MCM) technologies. Technologies featured in COTS 2 (Fig. 3b) include a Warp fuzzy logic coprocessor; CX2041 quick-turn application-specific integrated circuit (ASIC); amorphous silicon antifuse 22VP10 programmable array logic device (United Technologies Microelectronics Center); field-programmable gate arrays, for example, RT54SX16 and RH1020, and an antifuse-link MCM technology (Pico Systems).[2] COTS 2 will reduce uncertainties regarding space radiation of these devices, which will allow systems to exploit the increased performance of such components.[3]

COTS 3 (NASA)

The COTS 3 subexperiment (Fig. 3c) examines new photonics technologies, in particular optocoupler components that are under consideration for future NASA experiments. Motivation for COTS 3 came about due to problems experienced in certain newly installed optocouplers within the Hubble Space Telescope (HST) during its passage through the south Atlantic anomaly, which now prevent HST from operating there. These single-eventupsets did not occur in older optocouplers, which motivates further investigation of several different types of optocoupler devices, including those used in HST, by placing them into the COTS 3 experiment. In the COTS 3 experiment, a number of biased but nonilluminated optocouplers will be monitored for spurious pulse activity during operation through the radiation belts. Results will be compared with testing done at ground facilities, such as the Canadian TRIUMF facility.[4]

Dose Radiation Shielding Experiment (NASA/BMDO)

The dose radiation shielding experiment (DRSE) subexperiment provides a distribution of dosimeters in key spacecraft locations during the STRV-1d mission. The objectives of the DRSE are 1) to investigate a variety of shielding approaches, such as the RADCOAT technology[5§] and composite structure-basedtechniques and 2) to evaluate the total ionizing dose throughout STRV-1d spacecraft. A total of 24 individual monitoring nodes will be instrumented (with a total of 140 measurands), with each node containing a Jet Propulsion Laboratory invented RADMON[6] monolithic IC, augmented by an external Sandia National Laboratory (SNL) developed RADFET and thermometers. These devices provide a compact instrumentation approach for measuring total ionizing dose effects in conjunction with several different shielding filters. These data are essential for appropriate analysis of all ETB subexperiments, as well as collateral STRV-1d experiments (not a part of ETB), such as the BMDO-sponsored quantum-well infrared photodetector (QWIP) camera experiment.

Low-Power Electronics (DOD/AFRL)

Even as commercial industry, for example, laptop computers, continues to exploit advances in low-power microelectronics, this venue of research is particularly enabling in space systems, where every required joule of energy comes with a price tag. The low-power electronics (LPE) subexperiment (Fig. 4) demonstrates circuits 10–100 times more power efficient than current practice and examines, in particular, 1) reduction in feature size and 2) digital/analog integrated codesign and how these systems might perform in a synergistic environment. The heart of the subexperiment is an advanced instrument controller (AIC), built in a 0.35-μm, 3.3-V complementary metal oxide semiconductor (CMOS) technology for the central processing unit, two commercial memory devices (Hitachi 128 kbit $\times$ 8 SRAM and EEPROM), and a 70,000 device analog ASIC built in 2-μm CMOS (Orbit) process. The commercial devices were chosen based on components previously tested by NASA,[¶] where high resilience to SEP on read cycles had been demonstrated.[7] The AIC, developed for the NASA Deep Space 2 interplanetary mission, is packaged in a version of the high-density interconnect (HDI) MCM process[8] that employs a plastic substrate. The LPE experiment contains several dozen analog input channels, some of which will be compared with DHS analog measurements

[§] Data available online, for example, at http://www.spaceelectronics.com.

[¶] Data available online at http://flick.gsfc.nasa.gov/radhome.htm.

of LPE to track degradations that might occur with increased radiation.

Charge-Coupled Device (BMDO/AFRL)

Charge-coupled devices (CCDs) have significant potential applicability in a number of DOD missions, but these types of devices are notoriously susceptible to total ionizing dose in space missions. New types of CCDs, such as those under development at Lincoln Laboratory, are promising in that they have a higher degree of radiation tolerance than traditional CCD components. The CCD experiment (Fig. 5) contains a Lincoln Laboratory developed CCD (516×512 pixel arrangement) in a nonimaging configuration. A flood source illuminates five exposed regions of the detector (each containing 5×5 pixels) of the otherwise opaquely masked CCD, which is cooled to a nominal $-10°C$ operating temperature through a thermoelectric cooler. Two resistance-temperature detectors provide control loop sensing drive and instrumentation for follow-on calibration of data generated.

Transmit–Receive Antenna Module (AFRL)

In support of space-based radar research, extremely light-mass components must be developed and validated. The ground radar concept of a transmit–receive (TR) module is further augmented to include antennas in the novel space-based concept demonstrated in the TR antenna module (TRAM) subexperiment. A receive-only version of a TRAM system element (Fig. 6) comprises a subexperiment to examine the functional performance of a promising technology, which unites key radar components with several types of aggressive packaging, including plastic and flex-based forms of the HDI process. The novel use of HDI as an antenna, along with the high-performance nature of the controlled impedance interconnect structures for microwave applications, led to modules which performed to within 0.7 dB of theoretical projections. Demonstrating the representative TRAM structures in STRV-1d in a 1-year mission will provide an equivalent of nearly 10 years of exposure in a lower Earth orbit. The placement of the TRAM assembly on STRV-1d permits ground interaction through illumination of the satellite during operation, which provides verification of the antenna pattern fidelity over the STRV-1d mission.[9]

QWIP Detector (Canadian DREO)

The QWIP subexperiment (Fig. 7), not to be confused with the larger dedicated BMDO-sponsored QWIP camera experiment that is also resident on STRV-1d, is designed to explore radiation effects on a novel QWIP detector design. The subexperiment employs a passive radiator to cool the detector to 150 K. Measurements of the current voltage (I-V) curves of representative QWIP detector elements are gathered over the STRV-1d mission life under DHS control for postanalysis by Canadian researchers.

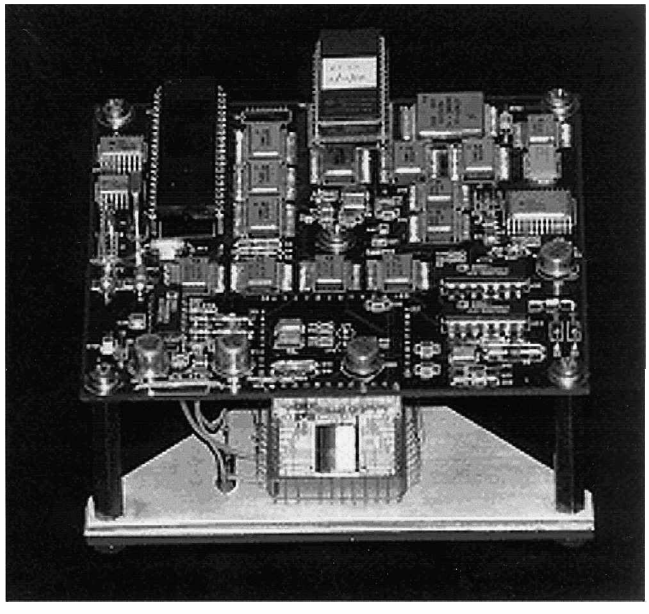


Fig. 5 CCD subexperiment.

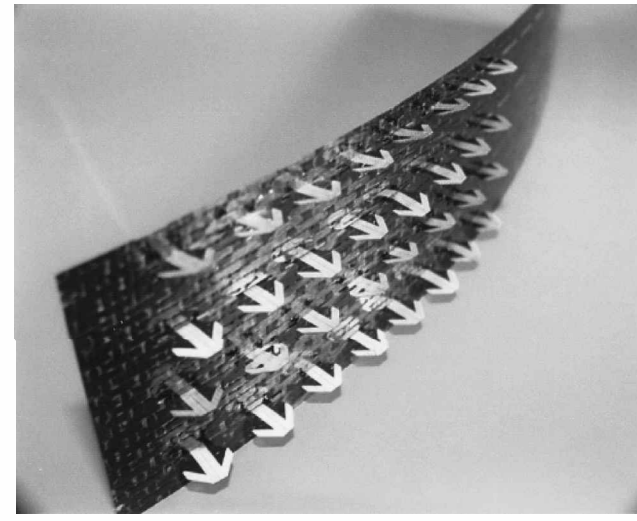


Fig. 6 TRAM subexperiment antenna module based on flexible HDI.

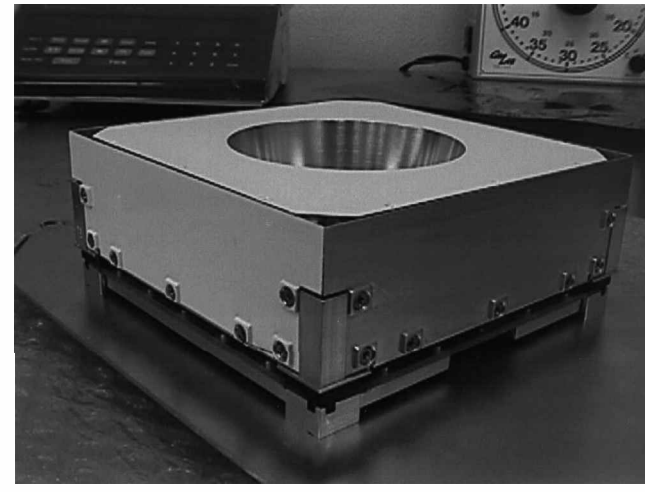
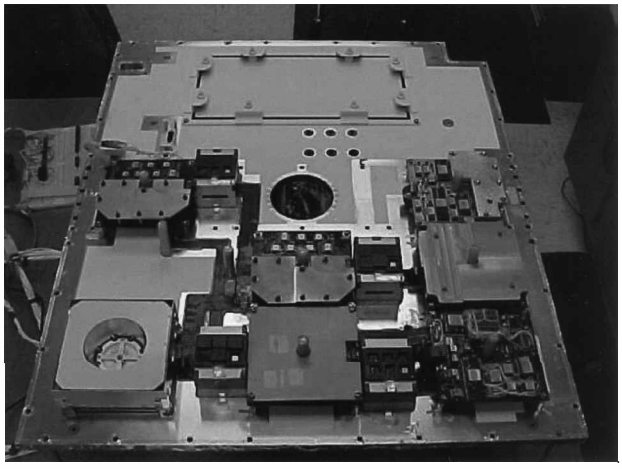


Fig. 7 QWIP subexperiment.

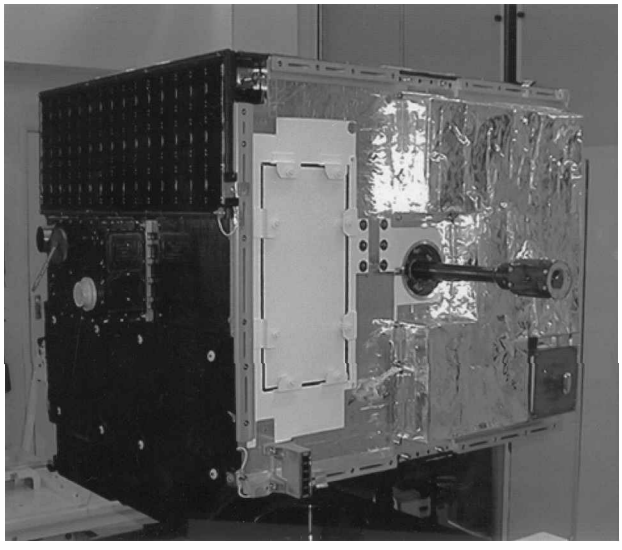
Common Requirements of ETB Subexperiments and Location on Top Panel

Each ETB subexperiment was provided with a number of stringent design requirements, which included fitting within a 10.8-cm square, with a ceiling height of less than 54 mm. The average mass of subexperiments was 250 g, and peak power consumption of any subexperiment was less than 5 W. All subexperiments were designed to interface to the DHS with a common 12-pin connector. The single interface provides an RS-422 format serial communications interface, three voltage supplies ($+5$ V and ± 12 V), two analog measurement channels, and an analog and dc ground connection. In principle, almost any experiment, with the exception of the TRAM experiment, could substitute for any other experiment through a simple software change. In this manner, ETB retains maximum flexibility for last minute changes to the manifest, include the addition of entirely new subexperiment hardware.

The relative locations of the subexperiments are shown in photographs of the STRV-1d spacecraft top panel in Fig. 8. Most subexperiments are located on the satellite top deck, which itself is an experimental multifunctional structure (MFS), which comprises a composite structure combined with an electrical interconnection manifold. The MFS replaces ordinary cable harnesses and bulky connectors with a copper–polyimide flexible circuitry system, similar to that used in the dashboards of automobiles since the 1960s. The arrangement of subexperiments on the top deck provide maximal exposure to radiation, and the total ionizing dose without shielding can



a)



b)

Fig. 8 Mounting location of subexperiments: a) top panel in early integration and b) assembled top panel (protruding boom) with all subexperiments except QWIP shrouded in insulation.

exceed 1 Mrad (Si). Figure 8a shows the juxtaposed arrangement of all subexperiments except TRAM on the top panel during integration testing on an engineering version of the final panel. Figure 8b shows the final integrated assembly. The subexperiments at this stage of integration are hidden beneath a thin shroud, which provides electrostatic shielding and emissivity control for the top surface of the satellite. Only the QWIP subexperiment is obviously exposed in the corner of the top panel. The TRAM and DRSE subexperiments are not placed on the top panel. Instead, the DRSE dosimeters are distributed throughout the spacecraft, whereas the TRAM antenna module is on one side of the spacecraft. As shown for some subexperiments, such as PHA (Fig. 2), additional shielding may be required to protect subexperiment-specific interface electronics. With proper shielding, the expected total ionizing dose exposure by components can be lower than 30 krad (Si) over a one-year mission life. The DHS, as well as the control electronics for the DRSE and TRAM subexperiments, are located underneath the top panel for additional radiation protection.

DHS Design and Development

The STRV-1d ETB DHS was based on a minimalist processor and processing concept, which, while efficient in size mass and power, provides expanded functionality over previous generations of the ETB, for example, the STRV-2 ETB. The ETB charter was originally defined around a concept for constructing a DOD-relevant, multiparticipatory radiation effects experiment, given strict limits

Table 1 ETB comparison

Feature	STRV-2 DHS	STRV-1d DHS
CPU, rad-hard	8086	80C31
Power, W	6	3
Serial communications interface ports	6 Custom, 1–1553 to spacecraft	11 RS-422
RAM, kB	512	1024
PROM, kB	32	32
Mass, kg	2	1.2
Analog support	None	16 Channels
Power to subexperiments, V	28	+5, ±12
Radiation tolerance, krad	100 (Si)	100 (Si)

for the ensemble (DHS plus all subexperiments) in mass (<4 kg) and power (10-W orbit average). To accommodate any reasonable allocation of mass and power for subexperiments, the DHS required extremely efficient engineering compared to the prior state of the art, represented by the STRV-2 DHS, which alone (without subexperiments) represented bulk in excess of 3 kg and consumed 6-W orbit average. As the STRV-1d DHS for ETB further evolved in response to subexperiment and spacecraft constraints, the addition of even more functionality was required compared to the previous STRV-2 design baseline. This expansion included the addition of individually regulated triplet power supplies for each subexperiment, the addition of analog sampling capability for most subexperiments, and a doubling of onboard data storage to 1 MB vs the 512 kB used in the STRV-2 DHS. The DHS design goals for STRV-1d are compared to STRV-2 DHS performance characteristics in Table 1.

Whereas creating a simple processor with a 3-W power budget is an almost trivial matter for terrestrial applications, the limited selection of component technologies for space-qualified, radiation-hardened applications made the task of designing the STRV-1d DHS particularly challenging. Some of the guiding principles and techniques that made it possible to converge on a tractable design are summarized:

1) The DHS did not require high throughput. Fundamentally, no reason existed to use a high-performance CPU. Especially in space, such processors typically are more efficient but still more power-hungry than a simple microcontroller could be.

2) The DHS employed gate array and MCM technology. In this case, the use of gate arrays and MCMs as a design method was a sensible proposition, especially due to the need to minimize size, mass, and power consumption.

3) The DHS did not use legacy solutions for their own sake. Strict adherence to a policy of legacy-motivated reuse of hardware and software concepts sometimes creates more problems in design, forcing the use of interfaces, components, and software constructs that deleteriously mitigate any advantage afforded by the legacy approach.

Despite these observations, it was an initial mandate that the STRV-1d DHS design be as nearly identical to the STRV-2 design as possible. A clone was out of the question because the STRV-2 DHS interface to the primary spacecraft processor employed a MIL-STD-1553 interface, whereas the STRV-1d spacecraft exploited a simpler communication protocol impressed on a bare-bones RS-422 interface. However, other barriers clearly precluded even a well-meaning clone of the STRV-2 design. First, power consumption in the STRV-2 design was so high that only 4 W would have been left over for remaining subexperiments using the STRV-2 DHS. Second, subexperiment participants for STRV-1d insisted on having multiple regulated power supplies and analog measurement services from the DHS. By contrast, an STRV-2 clone provided a single, unregulated 28-V supply to each subexperiment. Next, the protocol support needed in the STRV-2 DHS-to-subexperiment interface was based on a custom legacy protocol, sufficiently complicated to drive any subexperiment to employ a microprocessor. This complication would have precluded some subexperiments in the STRV-1d ETB from participation. Finally, the data storage and number of experiment interfaces were not adequate in the STRV-2 design.

In consideration of these constraints, a new DHS architecture was agreed to by BMDO and AFRL, a simplified representation

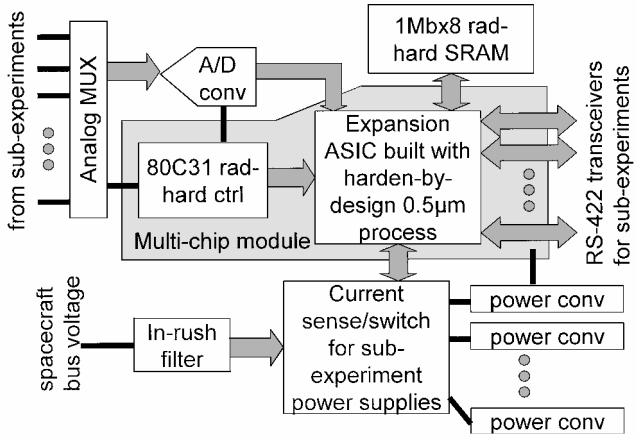


Fig. 9 Simplified DHS diagram.

of which appears in Fig. 9. The DHS is based around a special 8031/8051 8-bit microcontroller developed by SNL, which was very low power (125-mW average power under nominal conditions) and with a megarad radiation tolerance level. The various functional blocks of the DHS are discussed in more detail.

Control Section

The architecture of the DHS was organized around the principle that a simple microcontroller, the SNL 8031, a most effective choice for high-radiation space applications, could be extended in capability through the addition of logic resources. Because the DHS in its role definition would not perform any significant processing of data itself, the performance as measured in millions of instructions per second and, therefore, watts could be kept low. The idea of smart extensions to simple, "Spartan" processors was fundamental, and the introduction of gate array technology essential to the realization of an efficient DHS.

Gate arrays are customary and routine in ground applications, but their normally high expense keeps them out of the reach of normal experimenters. Although Actel field-programmable gate arrays (FPGAs) have been hardened to total dose, their current design is susceptible to single-event upset, which makes them a poor choice for an experiment concept where upsets to other parts of the experiment are not only expected but even desired. The DHS, based on such devices, could not "blink" while upsets were occurring throughout the experiment. In low-gate count designs, where implementations with substantial redundancy (where the redundant paths are spatially isolated) are involved, it is possible to employ FPGAs with single-event upset vulnerability. For example, triple modular redundancy and analogous methodologies can be exploited. Of course, in I/O bound applications, other factors bear on the decision between using FPGA and ASIC solutions. In these circumstances, the use of multiple FPGAs, even hardened ones, makes a poor fit. Fortunately, AFRL, working with the Mission Research Corporation, had developed a novel technique of hardening electronics through design, which was easily adapted to form low-gate-count, I/O-intensive custom components. As it turns out, careful examination of certain existing processes revealed that, through careful discipline in layout, it is possible to create extremely tolerant electronics for a relatively low cost. In fact, for the DHS, a 10,000 gate equivalent design was fabricated for about $10,000 (25 parts) by applying this harden by design approach, which is approximately $\frac{1}{10}$th the cost of some competing solutions.

As it turns out, the gate array implementation was relatively sparse from a logic resource perspective. Much of the functionality of the gate array was consumed in performing a multiplexing of 16 RS-422 channels into the single channel normally available on an 8051 CPU. Additionally, the gate array served as a bank-switching manager, which provided a method to expand the 8051 address space from 64 to 1024 kB (though access to no more than 64 kB can be given in any instant). As such, the gate array needs a larger quantity of I/O terminals than normal for a given size of silicon. This situation, referred to as pad limited, occurs when interconnect dominates logic in an IC design. The size of silicon ICs is often driven by the number of interconnections required at the package boundary. Had the DHS gate been built as a pad-limited design, the cost would have quadrupled because silicon fabrication processes charge by the square millimeter.

As such, gate array technology alone was not enough to secure the greatest economies. In the STRV-1d DHS, an HDI MCM was used to interconnect the gate array and 8051 CPU. This MCM, referred to as the basic instrument controller, comprised the essential core functionality of the ETB DHS for STRV-1d. Because the ASIC was built with a distributed I/O scheme, it would not be possible to use wire bonding. HDI, as a patterned overlay technology, permits easy access of I/O structures about the surface of an IC. The cost per square millimeter of HDI, even though at low volumes quite expensive, was still far less expensive than silicon, even in multiuser foundry concepts such as the metal oxide silicon implementation service.

Storage System

The DHS contains 32 kB of radiation-hardened programmable ROM (PROM) based on devices fabricated by Harris Semiconductor. The data storage system was originally designed for 128-kB capacity, on the initial assumption that adequate spacecraft storage was available and that ground contacts were frequent. In actuality, both assumptions were incorrect, and consequently the DHS had to be capable of buffering up to three days worth of science data. The DHS design features a number of radiation-hardened 128 kbit × 8 SRAM components fabricated by British Aerospace (formerly Lockheed Martin).

A backup solid-state recorder (SSR) was designed and partially built, based on a 1024-kB store of Hitachi 1-Mbit (128 kbit × 8) EEPROM devices and employing a double-sided chip-on-board packaging approach. The resultant design weighed approximately 1 oz and could be directly incorporated into the flight DHS. Because of concerns over adding another failure opportunity (a pessimistic way of viewing added features), its inclusion in the final DHS design was suspended, and the prototypes were assembled and shelved. Had they been included, these SSR units for STRV-1d might have given the DHS the ability to recover in many single-event disruptions (including discontinuous power-removal events caused by the spacecraft itself).

Power Management and Distribution

For the sake of robustness and fault tolerance, the ETB employs individual power convertors for each subexperiment and a separate converter for the DHS itself. The power converters, which are nominally 70% efficient, are compact switching supplies that generate ±12 V and +5 V to correspond with common requirements for analog and digital circuitry. A current sensing system exploits the DHS analog measurement system, and it monitors the power consumption on a continuous basis for anomalous conditions. Derated power metal-oxide-semiconductor field-effect transistors are employed in the design as solid-state power switches to activate each power supply.

Analog Measurement

Two Harris 9008 radiation-hardened 8-bit flash A/D convertors (A/DCs) are used in the DHS to provide monitoring channels for subexperiments. Each of the two subexperiment analog read channels are serviced by a separate A/DC.

DHS Software Design and Operational Concept

DHS models its operating concept after the STRV-2 DHS, which employs an event schedule table (EST) that governs the sequencing of subexperiment activity. The EST for the STRV-1d DHS comprises entries, which populate schedules. The use of a data-structure representation for schedule entries defines an experiment's operation within the context of a nominally 620-min orbit. The definition includes the experiment type, number of active channels, mode of operation, start time, and duration of operation. The schedule identification assigns the entry to a particular schedule profile, and a number of different profiles can be defined. Because of power limitations, only a subset of experiments can be operated at a particular

instant, and that set is defined by a particular schedule. Schedules are like scenarios, each of which can correspond to normal, low power, or special event case operations, for example, solar flare activity. Only one schedule can be active at any instant in time, and the sequence of schedules is itself defined by an entry in the EST table. The sequence of schedules, or schedule rotation, defines the routine pattern of DHS operation. When a special event occurs, a schedule defined for that event is called on, interrupting the normal rotation pattern. When that event has been cleared or disappears, the normal rotation pattern is resumed. The EST affords tremendous flexibility to the DHS. Whereas a default EST is burned into the permanent DHS memory, the EST can be reprogrammed in orbit by the spacecraft computer autonomously or under ground command.

In addition to the EST, a small feature table data structure is present in the DHS and is likened to a remote control switch panel. Many particular DHS functions can be affected using this feature table, such as which experiments should be serviced or ignored.

The DHS operates in a cyclic fashion, also referred to as a round-robin servicing approach. The DHS commands the subexperiments, one at a time, in a cycle that is repeated every 60 s. Each subexperiment is allotted 5 s to accommodate polling, commanding, data transfering, and sampling of one or both its analog channels. The DHS allows subexperiments to operate using three models: 1) processor based, 2) state-machine based, and 3) analog only. The processor-based subexperiments adhere to a strict protocol for communications. This protocol permits the issuance of mode change commands, viewing of status information, and reading of experiment data in the form of analog voltages on the two analog channels per subexperiment, as well as data packets of up to 255 B per time slice. In state-machine subexperiments, the DHS sends a poll character on its RS-422 interface to serve as a trigger, advancing a finite state machine to a new state. In such experiments, only analog information is recorded, with a reading on one or both channels corresponding to each advance of the state machine. In analog, only subexperiments, which are defined as experiments that do not exploit any communications with the DHS, the DHS reads one or both analog channels but performs no other operation on its RS-422 interface. In this manner very simple subexperiments, based only the requirement to read a voltage, can be accommodated.

Concepts for Future DHS Architectures

The STRV-1d experience has shown to date the viability of applying advanced technology and software design concepts to relatively simple controller concepts, when the explicit purpose of the controller is to broker satellite services and manage a diverse collection of resources that are commanded, monitored, and data logged. Even so, significant improvements are possible in next-generation electronics testbeds. This section reviews concepts to enable the construction of such ETBs.

More Efficient ETBs

New technologies, some of which are being demonstrated in the STRV-1d ETB, could be employed to build an ETB $\frac{1}{5}$th–$\frac{1}{10}$th the size of the present system, while reducing power consumption to well below $\frac{1}{2}$ W. One MCM implementation of an ETB-like system, the AIC used in the LPE experiment, features 32 analog input channels, 8 analog outputs, and 6 serial ports, while consuming less than 50-mW average power with a mass of 3 g. Unlike any previous ETB, the AIC can be reprogrammed in system, eliminating the need to burn PROMs or to deintegrate the unit for last minute code or data changes. Expansion of the AIC's 128 kB of RAM and nonvolatile memory can be readily done to achieve several megabytes of storage, more than adequate for many missions. Expansion of serial ports through redesign of the processing ASIC within the AIC and addition of high-density switchable power supplies could be effected to create a DHS smaller than a videocassette with superior performance characteristics to any previously constructed.

Improved Plug-and-Play in ETBs

The STRV-1d DHS provided a major improvement in plug-and-play compared to its precursor concept, which was effected through a combination of a simple physical interface and a flexible software design. In this manner, three completely different operating models were supported with the ability to accommodate easily a variety of subexperiments. Future designs could achieve even greater flexibility by employing a number of enhancements based on reconfigurable electronics approaches. First, the ability to provide discrete signals is desirable with software definable characteristics. Such an enhancement could create the opportunity to further simplify subexperiment design, for example, by allowing the DHS to generate finite state machines for subexperiments (state encoding on discrete lines). Second, the provision of D/A channels for subexperiments would allow the DHS to generate swept voltages across a given range, useful in many subexperiment designs. "Agile analog" is a further elaboration on analog channels, in which the gain and dc offset of each analog input and output could be specified, reducing the need for subexperiments to introduce some of the present analog conditioning circuitry. All of these concepts lead to DHS designs with a wider repertoire in flexible application to subexperiments that are simpler and quicker to build.

ETBs Without a Centralized DHS

With the miniaturization technologies discussed earlier and concepts in dynamically scheduled, real-time operating systems, it is possible to consider a new class of ETB, in which no central DHS exists. In such an ETB, a very tiny self-contained node processor/power convertor combination would be embedded within each subexperiment. The miniature node, based on a low-mass (approximately 50–75 g) assembly, would contain a processor, memory, at least six serial ports, a multitap power convertor, for example, 5 V and ± 12 V, and integral radiation monitors. Subexperiments attach to the node as done in present ETBs, and nodes would be linked through simple serial ports. The size of the node would be very small, approximately 3×4 cm, to minimize real estate impacts on individual subexperiments, and would operate at very low quiescent power levels (approximately 50 mW). Such a processor node could be based on several of the technologies used in the STRV-1d ETB, for example, AIC, RADMON, HDI.

Several important principles of the no-DHS ETB make this concept very attractive, especially for quick-turn missions. First, the ETB can be made as a self-organizing ensemble. Under such a scheme, a number of subexperiments can be strung together like Christmas tree lights, except that redundancy in the linkages can be employed, avoiding the potential to lose an entire chain with a single link failure. With the right applications code, the dynamic real-time operating system could establish a quorum of experiments as a distributed ETB, and communications to a spacecraft host computer could be effected redundantly. Under the concept of dynamically scheduled operating systems, stuck or defective nodes would be reset or disconnected and the node-specific tasks terminated. Protocols for distributing stored data could be established such that the loss of one or more subexperiments would not cause an unacceptable loss of data. Another attractive feature of an AIC-based distributed ETB is that each node is completely reprogrammable in situ, permitting last minutes changes in code or data. Such an ETB system is by nature quickly reconfigurable. With each node possessing its own radiation and temperature monitoring, dosimetry is automatically provided. Finally, the simple, low-complexity communications network, based on simple RS-422 ports and bus power, could be easily routed in many cases, permitting quick-response ETB installations on many satellites of opportunity. Conceivably, even without experiments, a number of such nodes could be "pasted" about a satellite, creating an instant distributed dosimetry system. The concept in one sense is an Internetlike approach to scalable systems, insulated from a number of single-point failures and dynamically elastic to expansion or other structural alterations in the network.

Conclusions

This paper addressed the design of the STRV-1d ETB DHS as a partnership between BMDO and AFRL. The guidance and funding provided by BMDO led to the development of a multiparticipatory program that, for a reasonable cost and quick-turn schedule, has established an ensemble of subexperiments that will allow

researchers to better understand the effects of radiation on cutting-edge microelectronics components and their associated processes. The harsh radiation environment of the STRV-1d spacecraft provides an excellent opportunity to compare accelerated versions of effects encountered in low Earth orbits with a variety of ground-testing results accumulated on components used in these subexperiments.

The DHS design represents a significant advance in efficiency in hardware and software design, leading to a system that effectively manages and collects data from a variety of experiments, while representing a very low overhead for the provision of those functions. The careful application of state-of-the-art technology resulted in this efficient implementation, which combines radiation-tolerant gate arrays, hardened by design, with MCM and modern software design. The operating model of the ETB contains tremendous flexibility to deal with changes in mission characteristics.

Finally, new concepts in DHS design were discussed. These concepts represent significant improvements over the state of the art in STRV-1d, leading ultimately to the concept of tiny, embeddable processors that contain an ability to self-organize fault-tolerant networks of subexperiments that can be arbitrarily distributed about a spacecraft. Such a DHS concept opens new possibilities in rapidly deployable ETBs that are responsive to short-term opportunities in spaceflight.

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